Supporting information

Multifunctional in-memory logics based on a dual-gate antiambipolar transistor toward non-von Neumann computing architecture

Yoshitaka Shingaya†, Takuya Iwasaki†, Ryoma Hayakawa†\*, Shu Nakaharai†, Kenji Watanabe‡, Takashi Taniguchi†, Junko Aimi§\*, Yutaka Wakayama†\*

†Research Center for Materials Nanoarchitectonics (MANA), National Institute for Materials Science (NIMS), 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan

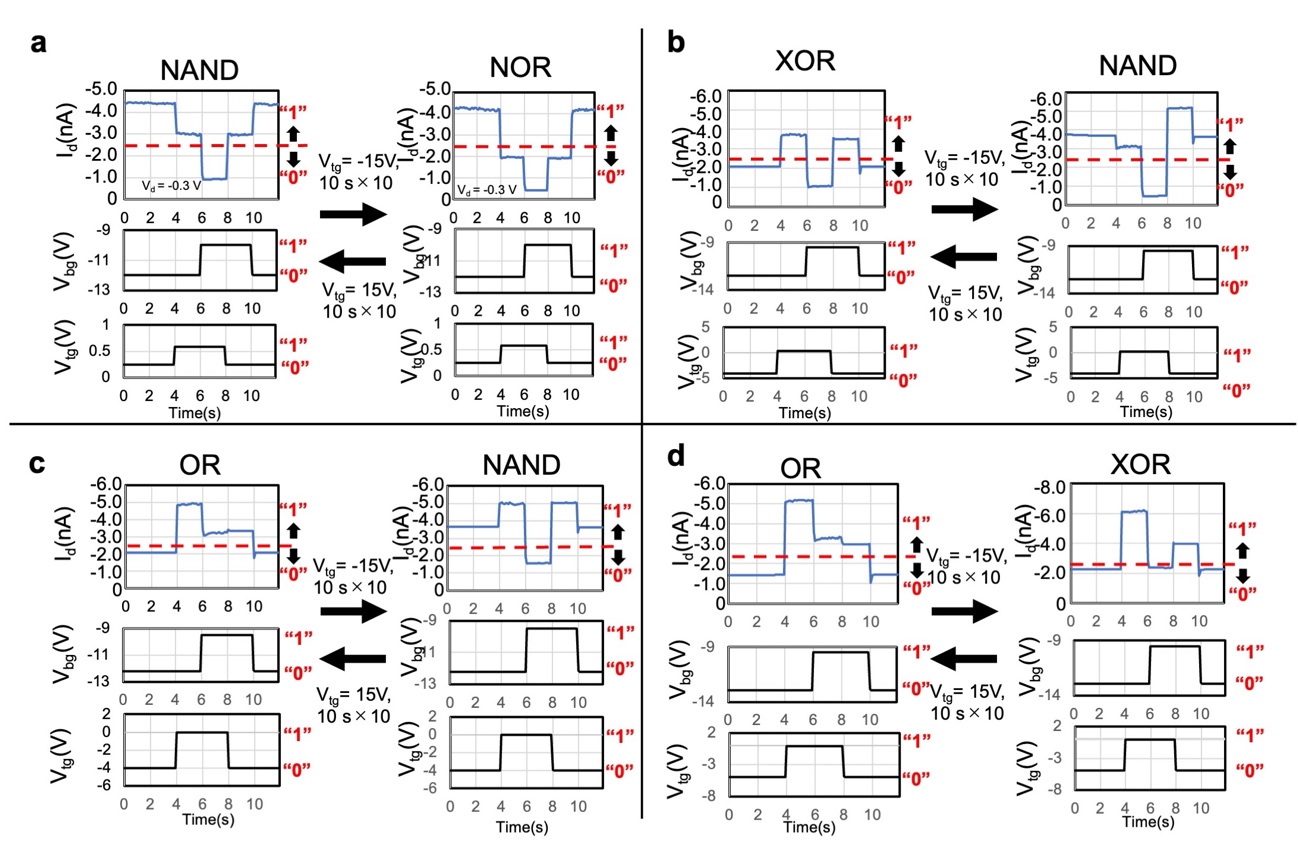
‡Research Center for Functional Materials, National Institute for Materials Science (NIMS), 1-1 Namiki, Tsukuba, Ibaraki 305-0044, Japan

§Research Center for Macromolecules and Biomaterials, National Institute for Materials Science (NIMS), 1-2-1 Sengen, Tsukuba, Ibaraki 305-0047, Japan

\*Email: HAYAKAWA.Ryoma@nims.go.jp, AIMI.Junko@nims.go.jp, WAKAYAMA.Yutaka@nims.go.jp

1. **Reconfigurable two-input logic circuits using non-volatile memory functions**

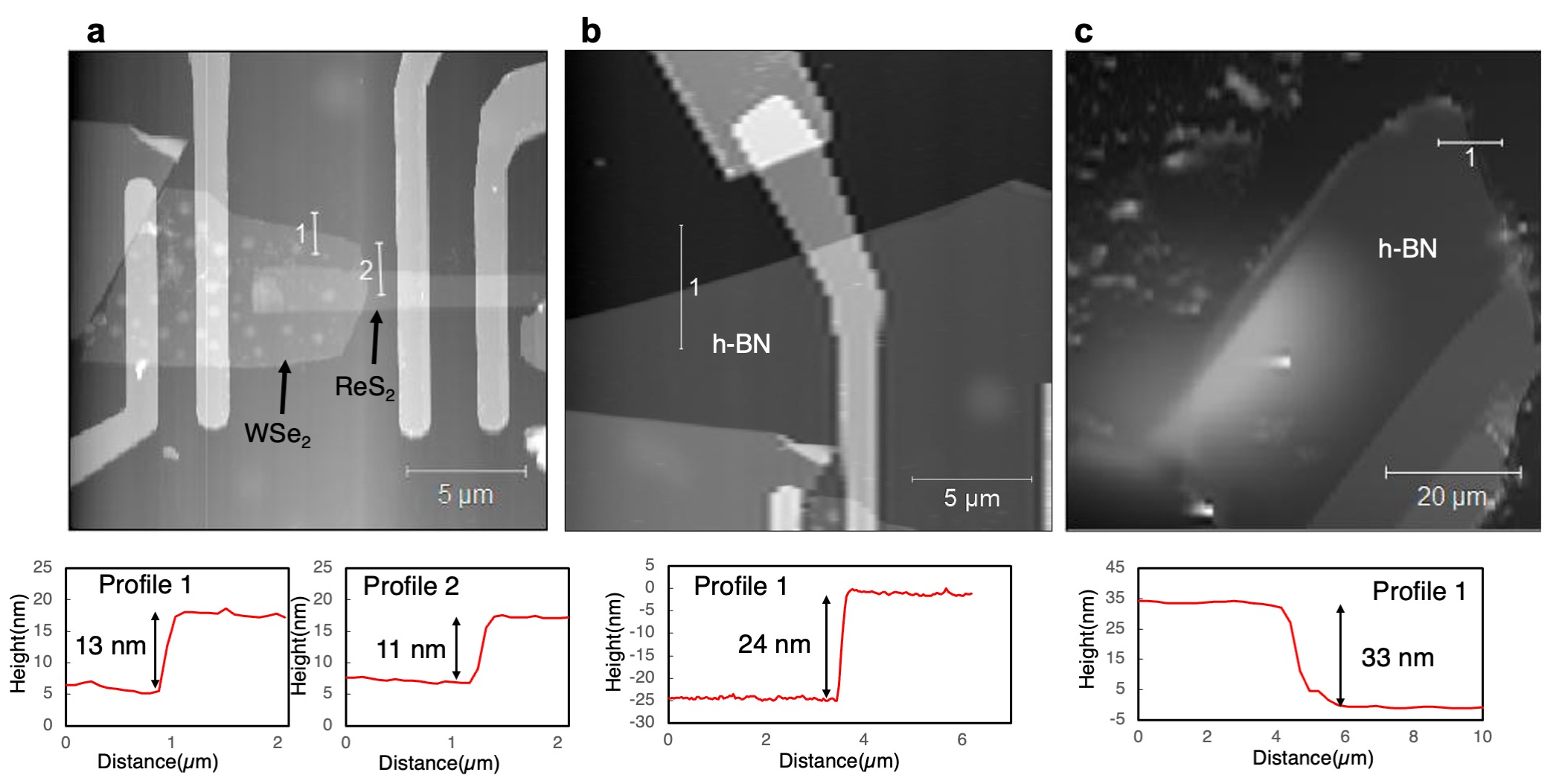
We demonstrated the electrical switching of two-input logic circuits by using the non-volatile memory effect of the polystyrene with a zinc phthalocyanine core (ZnPc-PS4). Figures S1a-S1d show four examples of the electrical switching of the two-input logic circuits, namely NAND/NOR, XOR/NAND, OR/NAND, and OR/XOR circuits. In all the circuits, the top-gate voltage (*V*tg) and the bottom-gate voltage (*V*bg) were employed as input signals 1 and 2, respectively. The output signal, “1” or “0”, is defined by whether |*I*d| is below or above 2.5 nA. Figure S1a shows the electrical conversion between the NAND and the NOR circuits. In the initial state, the low logic state “0” was output at (*V*tg, *V*bg) = (“1”, “1”). In contrast, *I*out exhibited the high logic state “1” for the other input signal combination. This operation corresponds to the NAND circuit. Then, a 10 times-negative *V*tg pulse (*V*tg = −15 V, *P*width = 10 s) induced conversion from the NAND to the NOR circuit. *I*d represented the high logic state “1” only when (*V*tg, *V*bg) were equal to (“0”, “0”), which is the same as that of the NOR circuit. Consequently, the NOR circuit was restored to a NAND circuit by applying a 10-times positive *V*tg pulse (*V*tg = 15 V, *P*width = 10 s). Importantly, the reconfiguration of the NAND and NOR circuits was realized without changing the input signals. In this manner, Fig. S1b-S1d show the electrical transitions between XOR and NAND, OR and NAND, and OR and XOR.



**Figure S1. Reconfigurable two-input logic circuits:** (a) NAND/ NOR, (b) XOR/NAND, (c) OR/NAND, and (d) OR/XOR.

1. **AFM observation of the fabricated device**

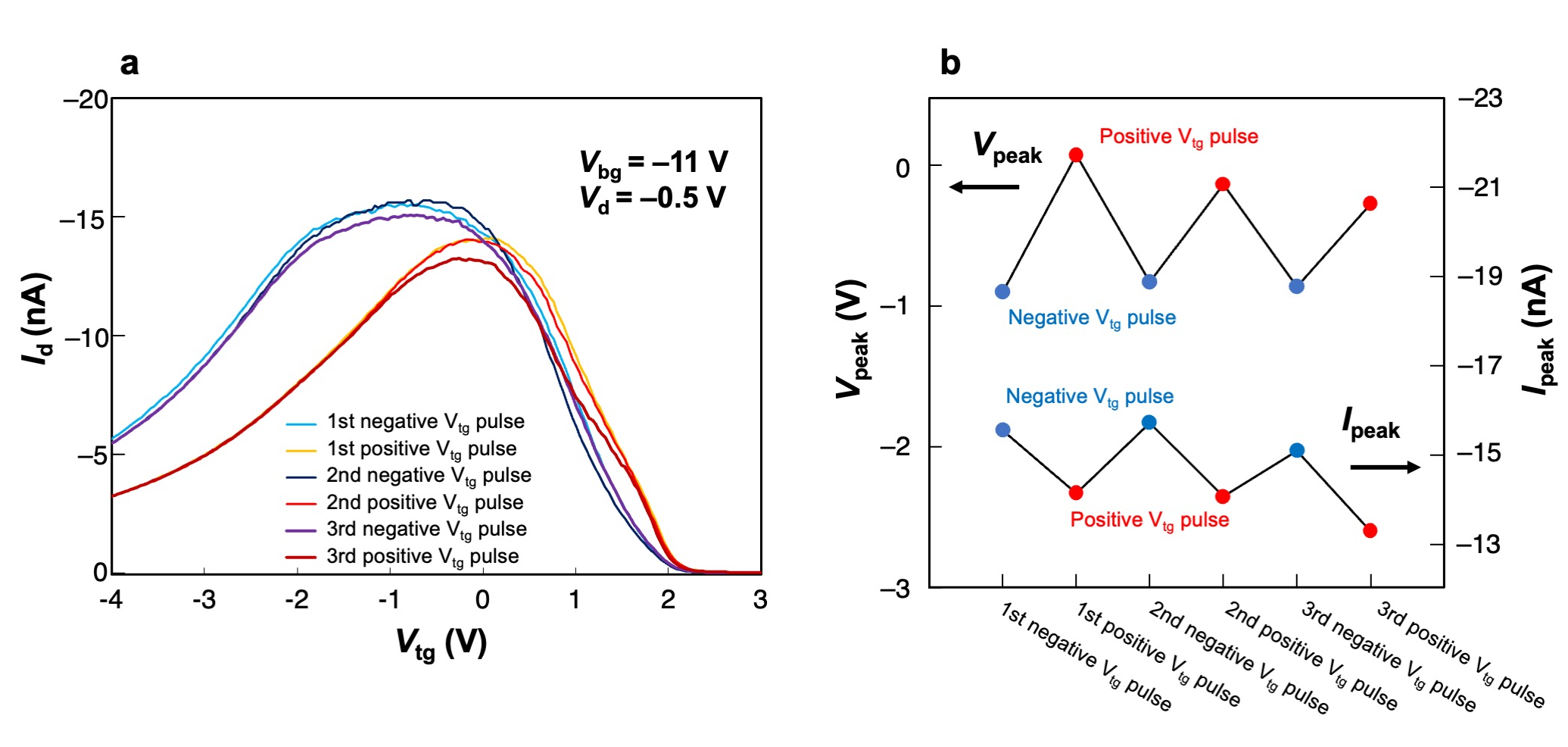
Atomic force microscope (AFM) observations were conducted to measure the thicknesses of the WSe2, ReS2 and h-BN layers (Figures S2a-c). Figure S2a shows an AFM image of the bottom-gate AAT before forming the top-gate configuration. The thicknesses of WSe2 and ReS2 were estimated to be 13 nm and 11 nm, respectively. The thickness of the bottom h-BN gate insulator was determined as 24 nm. Furthermore, the thickness of the top h-BN gate insulator was decided at 33 nm from the AFM image shown in Figure S2c.



**Figure S2.** AFM images of (a) WSe2 and ReS2 channel layers, (b) bottom and (c) top h-BN gate insulators

1. **Switching property of** **the dual-gate AAT with ZnPc-PS4 nano-floating gate**

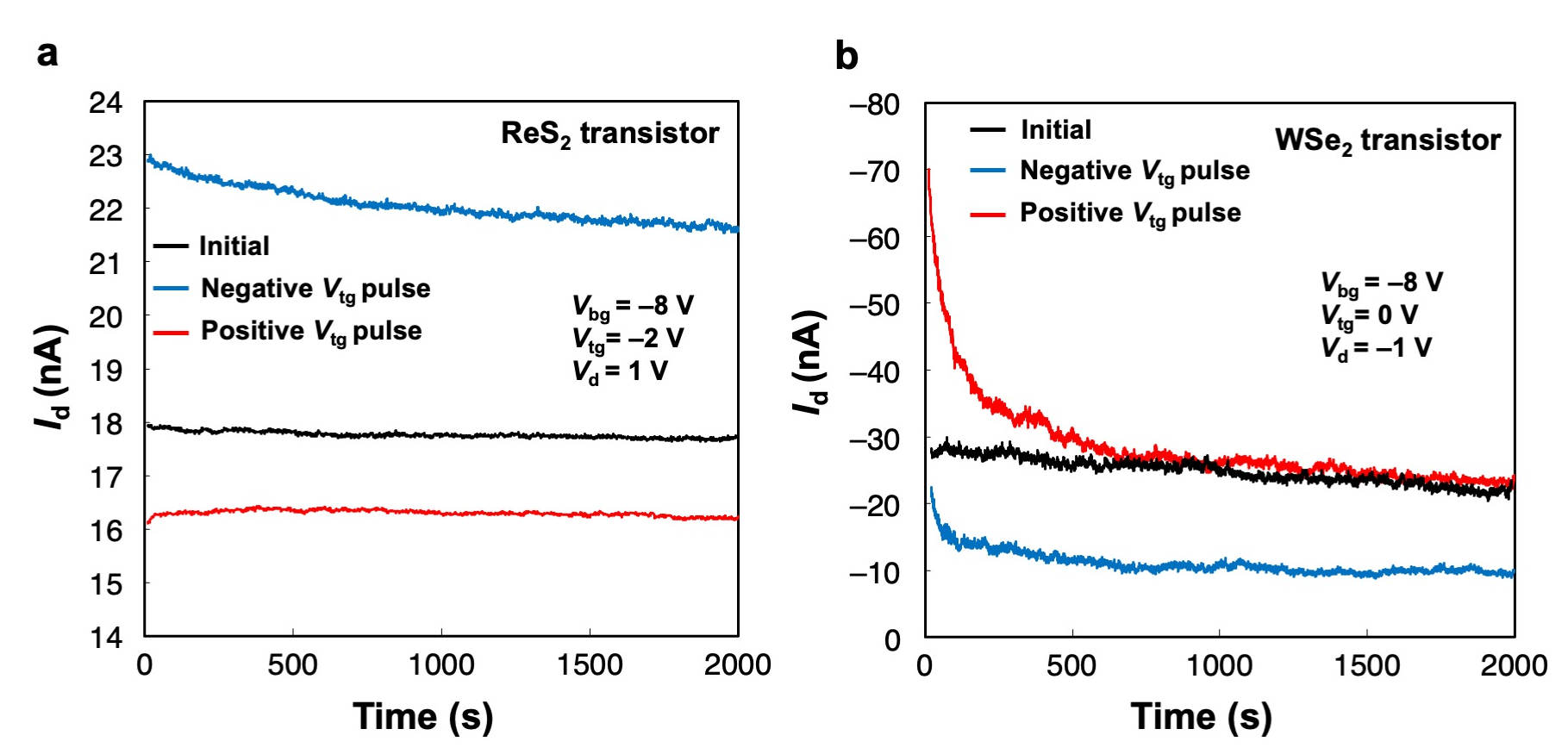
Figure S3a shows the transfer characteristics of the dual-gate AAT with the ZnPc-PS4 nano-floating gate after applying alternating negative *V*tg pulses (*V*tg = −15V, *P*width = 10 s, 5 times) and positive *V*tg pulses (*V*tg = 15V, *P*width = 10 s, 5 times). The variations in *V*peak and *I*peak, which are extracted from Figure S3a, are plotted as a function of the number of switching cycles in Figure S3b. The *V*peak and *I*peak values were almost constant after the repeated switching processes.



**Figure S3.** (a) Switching property of dual-gate AAT with nano-floating gate. (b) Variation of *V*peak and *I*peak values as a function of the number of switching cycles.

1. **Retention property of the ZnPc-PS4 nano-floating gate**

The retention property of the carrier-trapping states in the ZnPc-PS4 nano-floating gate was examined in ReS2 (Figure S4a) and WSe2 transistors (Figure S4b). The black lines in both figures show the variations of the drain currents in the initial states. In the ReS2 transistor (Figure S4a), the hole-trapping state (blue line) after applying a negative *V*tg pulse and the electron-trapping state (red line) after applying a positive *V*tg pulse were maintained for at least 2000 s. The WSe2 transistor also indicated a retention time of at least 2000 s for the hole trapping state (blue line in Figure S4b). Conversely, the trapped electrons in the ZnPc-PS4 layer were immediately released in the WSe2 transistor as indicated by the red line in Figure S4b.

****

**Figure S4.** Retention properties of the ZnPc-PS4 nano-floating gate in (a) ReS2 and (b) WSe2 transistors.